ACTIVE ELEMENT BIAS CIRCUIT FOR RF POWER TRANSISTOR INPUT

FIELD OF THE INVENTION

The present invention pertains generally to the field of radio frequency (RF) amplifier devices and, more specifically, to techniques for direct current (DC) biasing the input of a transistor used for amplifying a RF signal without incurring memory effect problems. By way of non-limiting example, the invention relates to RF power amplification circuits in wireless communication devices and networks.

BACKGROUND OF THE INVENTION

The use of transistor devices as signal amplifiers in wireless communication applications is well known. With the considerable recent growth in the demand for wireless services, such as personal communication services, the operating frequency of wireless networks has increased dramatically and is now well into the gigahertz (GHz) frequencies. At such high frequencies, Gallium Arsenide field effect transistors (GaAs FETs) have been preferred for power amplification applications, such as, e.g., use in mobile communication devices to provide power amplification for RF signals. In particular, GaAs FETs have a relatively high saturation power efficiency at frequencies of a few giga-hertz, e.g., at 2 GHZ.

When a GaAs FET is operated as a common source amplifier, such as in a metal-semiconductor field effect transistor (MESFET), the transistor gate is supplied with both the RF input signal to be amplified, as well as a DC bias voltage. Since the gate of a GaAs FET is a Shottky barrier, the relatively strong RF input signal power will rectify the Shottky barrier and

generate high positive gate current, which can destroy the transistor device. As a result, the DC bias supply circuitry is conventionally designed to prevent a high gate current.

By way of illustration, FIG. 1 illustrates a conventional power amplifier circuit 10 for amplifying a RF input signal, designated as "RF_{IN}," with the amplified output signal designated as "RF_{OUT}." The amplifier 10 includes a GaAs FET 15 operated as a common-source amplifier, with the input signal RF_{IN} applied to the gate terminal, the output signal RF_{OUT} received off the drain terminal, and the source terminal providing a relative ground for the common element current path. The amplifier 10 further comprises a gate bias circuit 20 for coupling a DC source 35 to the gate terminal of the GaAs FET 15. A DC blocking capacitor 25 is used in a conventional fashion to prevent the DC voltage from source 35 from passing upstream along the RF_{IN} signal path.

Within the gate bias circuit 20, the gate bias voltage from the DC source 35 is coupled to the gate of the GaAs FET 15 via a series connected, current limiting resistor 30. In particular, when a high gate current is generated by the RF_{IN} signal, the current will create a voltage drop between the gate and the DC source 35 across the resistor 30 and, thus, lower the gate current. The resistor 30 acts like a negative feedback to control the gate current and, thus, protect the transistor device 15. By way of further illustration, FIG. 2 is a graph of an exemplary gate current I_G versus power of the RF input signal RF_{IN} if the signal were connected directly to the bias voltage source 35 without the resistor 30. When the power of the RF input signal RF_{IN} is relatively low, the inherent body Shottky diode of the gate of the GaAs FET 15 is reversed biased and the gate current I_G is very small. As the power of the RF input signal RF_{IN} is increased, the gate current I_G increases in the negative direction from the drain to gate. This negative gate current I_G is caused by drain-to-gate breakdown of the GaAs FET 15. As the

power of the RF input signal RF_{IN} is further increased, the gate Shottky diode is rectified, i.e., forward biased, causing the gate current I_G to rapidly increase in the positive direction from the gate to the source. Heat generated by this positive gate current I_G, if allowed to increase unchecked, can destroy the GaAs FET device 15. Thus, the resistor 30 limits high positive gate current by producing a voltage drop between the voltage bias source 35 and the gate of the GaAs FET 15 when positive gate current flows through the resistor 30.

Returning to the amplifier 10 in FIG. 1, a relatively large value capacitor 40 is connected to ground between the DC voltage source 35 and the resistor 30 to create a ground path for the gate current. A shunt inductance 45 is coupled between the resistor 30 and the transistor gate to prevent the RF input signal RF_{IN} from flowing through the capacitor 40. In the illustrated embodiment, the shunt inductance 45 comprises a quarter-wavelength (¼ λ) stub, where λ is the wavelength of the fundamental carrier frequency f_0 of the RF input signal, e.g., 2 GHz, in parallel with a relatively small bypass capacitor 50 shorted to ground. The ¼ λ stub appears as a short circuit to the RF input signal RF_{IN}, while providing a low (essentially purely resistive) impedance path for the DC bias voltage source 35. The bypass capacitor 50 provides a short to ground for the RF_{IN} signal and an open circuit for the voltage bias source 35, and is invisible to the gate current of the GaAs FET 15. Therefore, the ¼ λ stub 45 passes the voltage bias source 35 to the gate terminal of the GaAs FET 15, while blocking the RF input signal RF_{IN} from entering the gate bias circuit 20. Alternately, a RF choke could be used instead of the ¼λ stub for providing the shunt inductance 45.

Notably, the voltage drop across the resistor 30 varies the gate bias voltage when there is positive gate current. This variation in the gate bias voltage varies the bias condition of the amplifier 10, which impacts the amplifier's performance, e.g., gain, output power, impedance

matching, etc. It would be desirable to correct for this non-linear distortion by using known predistortion techniques. However, because the RF input signal RF_{IN} is typically amplitude modulated, a time-varying amplitude envelope is impressed on the RF input signal. When this time-varying amplitude is large enough to forward bias the Shottky diode of the gate of the GaAs FET 15, positive gate current is produced. The variation in the gate bias voltage will depend not only on the instantaneous gate current, but on the history of the gate current leading up to the instantaneous gate current, as well. This phenomenon, commonly known as a "memory effect," is caused by the voltage bias capacitor 40 forming a RC circuit with resistor 30, which limits the response time of the gate voltage circuit 20 to changes in the gate current. When the frequency of the gate current exceeds $1/(2\pi RC)$, the gate bias circuit 20 can not change the gate bias voltage fast enough to follow instantaneous changes in the gate current. As such, the ability of predistortion to correct the distortion of the RF output signal caused by the variation in the gate bias voltage in conventional RF amplifier circuits is limited.

SUMMARY OF THE INVENTION

In accordance with a first aspect of the invention, a circuit is provided for gate biasing a transistor used for amplifying an RF signal in a wireless communication device, a handset or radio base station.

In one embodiment, the bias circuit includes an active element in series with a resistor in a DC bias circuit. The active element provides a relatively low impedance over a bandwidth comparable to an amplitude modulation bandwidth of the RF signal, such that a DC bias voltage applied at the active element has a fixed DC voltage at the resistor input, i.e., without any memory effect, thereby allowing for improved predistortion compensation.

Other aspects and features of the present invention will become apparent from consideration of the following description made in conjunction with the accompanying drawings of a preferred embodiment.

BREIF DESCRIPTION OF THE DRAWINGS

The drawings illustrate both the design and utility of a preferred embodiment of the invention, presented in contrast with a prior art embodiment for better illustration, wherein:

FIG. 1 is a circuit schematic diagram of a conventional power amplifier.

FIG. 2 is a graph showing the gate current of a GaAs FET versus power level of an RF input signal in a power amplifier circuit without a gate current limiting resistor.

FIG. 3 is a circuit schematic diagram of a power amplifier according to one embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In accordance with the a general aspect of the invention, the passive capacitor used for providing a ground path for the gate current in conjunction with the current limiting resistor in conventional gate biasing circuits (e.g., capacitor 40 in the gate biasing circuit 20 of FIG. 1) is replaced with an active circuit element which provides a low output impedance over the operating frequency bandwidth of the RF input signal. In this manner, the gate current will see only a purely resistive load throughout the signal frequency bandwidth, without also further introducing unwanted memory effect into the biasing circuit.

Importantly, while the concepts and advantages of the invention will now be described in accordance with an embodiment directed to gate biasing of a GaAs FET, the invention may be equally employed in biasing circuits for other RF devices having drive dependent gate currents. By way of non-limiting examples, devices such as a GaAs pHEMT may also have drive dependent gate currents. Although bi-polar transistors do not have gates, and instead receive the RF input signal at their base (with a common emitter configuration), or emitter (with a common base configuration), they still require DC input biasing and have the same current limiting resistor configuration as the GaAs FET embodiments described herein. Further devices that may be used in RF amplifier circuits include heterojunction bi-polar transistors ("HBTs") which do not have a gate per se, but still require DC biasing of the RF input signal and can benefit by employing an active element in conjunction with a current limiting resistor to prevent memory effect in the biasing circuit. Thus, the invention is not limited to gate biasing circuits, per se.

FIG. 3 shows a circuit schematic of a RF amplifier circuit 110 constructed in accordance with one embodiment of the invention. The amplifier 110 includes a GaAs FET 115 operated as a common-source amplifier, with the input signal RF_{IN} applied to the gate terminal, the output

signal RF_{OUT} received off the drain terminal, and the source terminal providing a relative ground for the common element current path. The amplifier 110 further comprises a gate bias circuit 120 for coupling a DC source 135 to the gate terminal of the GaAs FET 115. A DC blocking capacitor 125 is used in a conventional fashion to prevent the DC voltage from source 35 from passing upstream along the RF_{IN} signal path.

As in the conventional gate bias circuit 20 of amplifier circuit 10 in FIG. 1, the gate bias voltage from the DC source 135 is coupled to the gate of the GaAs FET 115 via a series connected, current limiting resistor 130, which provides a negative feedback to control the gate current and, thus, protect the transistor device 115. As also in the conventional gate bias circuit 20, a shunt inductance 145 and bypass capacitor 150 are coupled between the resistor 130 and the gate of transistor 115 to short circuit the RF input signal RF_{IN}, while providing a low (essentially purely resistive) impedance path for the DC bias voltage source 135. The shunt inductance 145, which may comprise a quarter-wavelength (¼ λ) stub, or alternatively, an RF choke, passes the DC voltage from source 135 to the gate of the GaAs FET 115, while blocking the RF input signal RF_{IN} from entering the gate bias circuit 120.

In accordance with the invention, the passive voltage bias capacitor 40 of conventional biasing circuit 20 is replaced in circuit 120 with an active element 140 connected in series between the voltage bias source 135 and the current limiting resistor 130. In the illustrated embodiment, the active element circuit 140 comprises an operational amplifier (op amp) 155 having a negative input terminal, a positive input terminal and a single-ended output. A first resistor 160 is connected between the voltage bias source 135 and the negative input terminal of the op amp 155, and a second resistor 165 is connected between the negative input terminal and

the output of the op amp 155. The positive input terminal of the op amp 155 is connected to ground and the output is connected to the current limiting resistor 130.

The op amp 155 preferably has high internal impedance at its two input terminals so that negligible current flows into the negative input terminal from the voltage bias source 135. That way, almost all of the current passing through resistor 160 from the voltage bias source 135 also flows through resistors 165 and 130. In addition, the op amp 155, preferably, has a relative low output impedance and a high gain. The arrangement of resistor 160 ("R1"), resistor 165 ("R2"), and the op amp 155 forms an inverting amplifier circuit having an output voltage, V_{out} approximately equal to

$$V_{out} = -(R2/R1)*V_{bias}$$

where V_{bias} is the voltage of the voltage bias source 135. This approximation is good when the gain of the op amp 155 is a few orders of magnitude larger than R2/R1. When negligible current flows through the resistor 130, the gate bias voltage at the gate of transistor 115 is approximately equal to the output voltage V_{out} of the active element circuit 140. The actial value of resistors 160 and 165 are dependent on the desired operating characteristics of the amplifier circuit 110. For example, when resistors 160 and 165 have equal resistance, a gate voltage bias of -1.5 V can be achieved by using a voltage bias V_{bias} of 1.5 V.

The op amp 155 preferably has a frequency bandwidth that at least encompasses the bandwidth of the gate current of the transistor 115, such that that the output impedance of the op amp 155 remains purely resistive throughout the bandwidth of the gate current. For example, for a gate current bandwidth of DC to 10 MHz, the op amp 155 can have a bandwidth of DC to 30 MHz. This way, the output impedance of the gate bias circuit 120 seen at the gate of transistor 115 is purely resistive throughout the bandwidth of the gate current. As a result, the variation in

the gate bias voltage produced by the gate bias circuit 120 only depends on the instantaneous gate current, without the undesirable memory effect associated with the voltage bias capacitor 40 of the prior art biasing circuit 20. This enables the distortion in the RF output signal caused by the variation in the gate bias current to be corrected using known predistortion techniques.

While various embodiments of the application have been described, it will be apparent to those of ordinary skill in the art that many embodiments and implementations are possible that are within the scope of the present invention.

For example, the op amp 155 and resistors 160 and 165 of the active element circuit 140 may be arranged to form a non-inverting amplifier, instead of the inverting amplifier. Notably, in alternate embodiments, the active element circuit 140 may comprise different circuit components, while still providing relatively low output impedance throughout the bandwidth of the gate current of transistor 115. By way of one example, the op amp 155 may be replaced by a suitable arrangement of transistors.

Therefore, the invention is not to be restricted or limited except in accordance with the following claims and their equivalents.